FEB 28 2005

FORM PTO-1449

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. 1875.0560002	APPLICATION NO. 09/844,296
INVENTORS BUCHWALD et al.	
FILING DATE April 30, 2001	ART UNIT 2634

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
JP	AA1	5,396,224	03/1995	Dukes et al.			
JP	AB1	5,550,546	08/1996	Noneman et al.			
JP	AC1	5,768,268	06/1998	Kline et al.			
JP	AD1	5,822,143	10/1998	Cloke et al.			
JP	AE1	5,881,107	03/1999	Termerinac et al.			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
JP	AF1	EP 1 006 697	06/2000	EP			N/A
JP	AG1	EP 1 139 619	10/2001	EP			N/A
JP	AH1	WO 01/29991	04/2001	WO			N/A

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JP	AI1	Black, Jr., W. and Hodges, D., "Time Interleaved Converter Arrays," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. SC-15, No. 6, December 1980, pages 1022-1029.
JP	AJ1	Conroy, C. et al., "An 8-b 85-MS/s Parallel Pipeline A/D Converter in 1-µm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 28, No. 4, April 1993, pages 447-454.
JP	AK1	Dally, W. and Poulton, J., "Transmitter Equalization for 4Gb/s Signalling," *Proceedings of Hot Interconnects IV*, Palo Alto, CA, 1996, 10 pages.
JP	AL1	Ellersick, W. et al., "A Serial-Link Transceiver Based on 8GSample/s A/D and D/A Converters in 0.25µm CMOS," *IEEE International Solid-State Circuits Conference*, IEEE, 2001, page 58-59 and 430.
JP	AM1	Ellersick, W. et al., "GAD: A 12-GS/s CMOS 4-bit A/D Converter for an Equalized Multi-Level Link," *Symposium on VLSI Circuits Digest of Technical Papers*, 1999, pages 49-52.
JP	AN1	Eklund, J-E. and Gustafsson, F., "Digital Offset Compensation of Time-Interleaved ADC Using Random Chopper Sampling," *IEEE International Symposium on Circuits and Systems*, IEEE, May 28-31, 2000, pages III-447 thru III-450.

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JP	AA2	5,949,820	09/1999	Shih et al.			
JP	AB2	6,005,445	12/1999	Katakura			
JP	AC2	6,009,534	12/1999	Chiu et al.			
JP	AD2	6,038,269	03/2000	Raghavan			
JP	AE2	6,134,268	10/2000	McCoy			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
JP	AF2	WO 01/54317	07/2001	WO			N/A
JP	AG2	WO 01/65788	09/2001	WO			N/A
JP	AH2	WO 01/84702	11/2001	WO			N/A

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JP	AI2	Fu, D. et al., "A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," IEEE Journal of Solid-State Circuits, IEEE, Vol. 33, No. 12, December 1998, pages 1904-1911.
JP	AJ2	Guizani, M. and Al-Ali, A., "PC-Compatible Optical Data Acquisition Unit," Instrumentation and Measurement Technology Conference, IEEE, May 10-12, 1994, pages 1099-1102.
JP	AK2	Jenq, Y.-C., "Digital Spectra of Nonuniformly Sampled Signals: A Robust Sampling Time Offset Estimation Algorithm for Ultra High-Speed Waveform Digitizers Using Interleaving" Transactions on Instrumentation and Measurement, IEEE, Vol. 39, No. 1, February 1990, pp. 71-75.
JP	AL2	Mason, R. and Taylor, J.T., "High-Speed Electro-Optic Analogue to Digital Converters," IEEE International Symposium on Circuits and Systems, IEEE, 1993, pages 1081-1084.
JP	AM2	Niewczas, P. et al., "Error Analysis of an Optical Current Transducer Operating with a Digital Signal Processing System," IEEE Transactions on Instrumentation and Measurement, IEEE, Vol. 49, No. 6, December 2000, pages 1254-1259.
JP	AN2	Petraglia, A. and Mitra, S., "Analysis of Mismatch Effects Among A/D Converters in a Time-Interleaved Waveform Digitizer," IEEE Transactions on Instrumentation and Measurement, IEEE, Vol. 40, No. 5, October 1991, pages 831-835.

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JP	AA3	6,329,859 B1	12/2001	Wu			
JP	AB3	6,359,486 B1	03/2002	Chen			
JP	AC3	6,397,048 B1	05/2002	Toda			
JP	AD3	6,404,525 B1	06/2002	Shimomoura et al.			
JP	AE3	6,498,694 B1	12/2002	Shah			

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JP	AF3	WO 01/84724	11/2001	WO			N/A
JP	AG3	WO 02/13424	02/2002	WO			N/A
JP	AH3	WO 02/071616	09/2002	WO			N/A

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JP	AI3	Sauer-Greff, W. et al., Maximum-Likelihood Sequence Estimation of Nonlinear Channels in High-Speed Optical Fiber Systems, April 6, 2001, Retrieved from the Internet at http://www.ftw.at/Dokumente/010406a.pdf, 29 pages.
JP	AJ3	Williamson, R.C. et al., "Effects of Crosstalk in Demulitplexers for Photonic Analog-to-Digital Converters," Journal of Lightwave Technology, IEEE, Vol. 19, No. 2, February 2001, pages 230-236.
JP	AK3	Yang, C-K., Design Techniques for High-Speed Chip-to-Chip Links, Retrieved from the Internet at http://web.doe.carleton.ca/courses/97578/topic5/Tutorial_SerialLink.pdf, 31 pages.
JP	AL3	Yang, C-K. et al., "A Serial-Link Transceiver Based on 8-Gsamples/s A/D and D/A Converters in 0.25-μm CMOS," IEEE Journal of Solid-State Circuits, IEEE, Vol. 36, No. 11, November 2001, pages 1684-1692.
JP	AM3	Zuoxi, T., "Implementation of a Digital Multibeam Receiver Based on TMS320C80 for Laser Optoacoustic Remote Sensing," Proceedings of ICSP2000, IEEE, 2000, pages 2082-2084.
JP	AN3	Agazzi, O. and Lenosky, T., Algorithm to Postprocess Measured Data, IEEE 802.3ae Equalization Ad Hoc Group, January 10, 2001, 11 pages.

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		ATTY. DOCKET NO. 1875.0560002	APPLICATION NO. 09/844,296
FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT		INVENTORS BUCHWALD *et al.*	
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JP	AA4	6,509,773 B2	01/2003	Buchwald *et al.*			
JP	AB4	6,621,862 B1	09/2003	Dabell			
JP	AC4	6,791,388 B2	09/2004	Buchwald *et al.*			
JP	AD4	2002/0012152 A1	01/2002	Agazzi *et al.*			
JP	AE4	2002/0034222 A1	03/2002	Buchwald *et al.*			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AF4						Yes No
	AG4						Yes No
	AH4						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

JP	AI4	Agazzi, O., *A Link Model for Equalized Optical Receivers*, IEEE 802.3ae Equalization Ad Hoc Group, March 11, 2001, 30 pages.
JP	AJ4	Agazzi, O. *et al.*, *DSP-Based Equalization for Optical Channels: Feasibility of a VLSI Implementation*, IEEE 802.3ae, New Orleans, September 12-14, 2000, 39 pages.
JP	AK4	Agazzi, O. *et al.*, *Interim Observations on Multimode Optical Channels*, IEEE 802.3ae - Equalization Ad Hoc, Tampa, November 5, 2000, 29 pages.
JP	AL4	Agazzi, O. *et al.*, *Measurements of DMD-Challenged Fibers at 3.125Gb/s*, IEEE 802.3ae Equalization Ad Hoc, January 10, 2001, 33 pages.
JP	AM4	Agazzi, O. and Lenosky, T., "Measurement of Non-Stationarity of 10 Gb/s Multimode Fiber Links," November 24, 2000, 5 pages.
JP	AN4	Agazzi, O., *10 Gb/s PMD Using PAM-5 Modulation*, IEEE 802.3, Dallas, January 18-20, 2000, 19 pages.

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ꟼ	AA5	2002/0039395 A1	04/2002	Buchwald et al.			
ꟼ	AB5	2002/0044618 A1	04/2002	Buchwald et al.			
ꟼ	AC5	2002/0080898 A1	06/2002	Agazzi et al.			
ꟼ	AD5	2003/0086515 A1	05/2003	Trans et al.			
ꟼ	AE5	2004/0212416 A1	10/2004	Buchwald et al.			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AF5						Yes No
	AG5						Yes No
	AH5						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

ꟼ	AI5	Agazzi, O. et al., *10 Gb/s PMD Using PAM-5 Trellis Coded Modulation*, IEEE 802.3, Alburquerque, March 6-10, 2000, 38 pages.
ꟼ	AJ5	Bhatt, V., *Equalization Ad Hoc Concluding Report*, IEEE P802.3ae Plenary, March 2001, 12 pages.
ꟼ	AK5	Bingham, J.A.C., "Multicarrier Modulation for Data Transmission: An Idea Whose Time Has Come," *IEEE Communications Magazine*, IEEE, Vol. 28, No. 5, pages 5-8 and 11-14.
ꟼ	AL5	Chiddix, J. et al., "AM Video on Fiber in CATV Systems: Need and Implementation," *IEEE Journal on Selected Areas in Communications*, IEEE, Vol. 8, No. 7, September 1990, pages 1229-1239.
ꟼ	AM5	Darcie, T., "Subcarrier Multiplexing for Lightwave Networks and Video Distribution Systems," *IEEE Journal on Selected Areas in Communications*, IEEE, Vol. 8, No. 7, September 1990, pages 1240-1248.
ꟼ	AN5	Fettweis, G., "High-Rate Viterbi Processor: A Systolic Array Solution," *IEEE Journal on Selected Areas in Communications*, IEEE, Vol. 8, No. 8, October 1990, pages 1520-1534.

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	AA6						
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	AC6						
	AD6						
	AE6						

FOREIGN PATENT DOCUMENTS

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	AF6						Yes No
	AG6						Yes No
	AH6						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

JP	AI6	Fettweis, G., "Parallel Viterbi Algorithm Implementation: Breaking the ACS-Bottleneck," *IEEE Transactions on Communications*, IEEE, Vol. 37, No. 8, August 1989, pages 785-790.
JP	AJ6	Forney, Jr., G.D., "The Viterbi Algorithm," *Proceedings of the IEEE*, IEEE, Vol 61, No. 3, March 1973, pages 268-278.
JP	AK6	Frazier, H., *IEEE 802.3 Higher Speed Study Group*, IEEE 802.3 HSSG, Kauai, Hawaii, November 9, 1999, 24 pages.
JP	AL6	Giaretta, G. and Lenosky, T., *Adaptive Equalization of DMD Challenged Multimode Fiber at 1300 mm*, IEEE P802.3ae Plenary, March 11, 2001, 10 pages.
JP	AM6	Hatamian, M. *et al.*, "Design Considerations for Gigabit Ethernet 1000Base-T Twisted Pair Transceivers," *IEEE 1998 Custom Integrated Circuits Conference*, IEEE, 1998, pages 335-342.
JP	AN6	Isaacs, M *et al.*, *Measurements of Fiber Responses at 5 Gb/s Data Rate Using 850nm VCSELs*, IEEE 802.3ae Equalization Ad Hoc, March 11, 2001, 18 pages.

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	AA7						
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	AE7						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AF7						Yes No
	AG7						Yes No
	AH7						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

JP	AI7	Kanno, N. and Ito, K., "Fiber-Optic Subcarrier Multiplexing Video Transport Employing Multilevel QAM," *IEEE Journal on Selected Areas in Communications*, IEEE, Vol. 8, No. 7, September 1990, pages 1313-1319.
JP	AJ7	Kasper, B.L., "Equalization of Multimode Optical Fiber Systems," *The Bell System Technical Journal*, American Telephone and Telegraph Company, Vol. 61, No. 7, September 1982, pages 1367-1388.
JP	AK7	Kasturia, S. and Winters, J., "Techniques for High-Speed Implementation of Nonlinear Cancellation," *IEEE Journal on Selected Areas in Communications*, IEEE, Vol. 9, No. 5, June 1991, pages 711-717.
JP	AL7	Lenosky, T., *A Unified Method of Calculating PMD-induced Pulse Broadening*, IEEE 802.3ae Equalization Ad Hoc Meeting, Tampa, Florida, November 5, 2000, 8 pages.
JP	AM7	Lenosky, T. and Giaretta, G., *Five Gb/s Multimode DMD at 850 nm: Real-Time Data and Equalizer Simulations*, Finisar Corporation, March 11, 2001, 13 pages.
JP	AN7	Lenosky, T. et al., *Measurements of DMD-Challenged Fibers at 850nm and 2Gb/s Data Rate*, IEEE 802.3ae - Equalization Ad Hoc Group, January 10, 2001, 21 pages.

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	AA8						
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	AF8						Yes No
	AG8						Yes No
	AH8						Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

JP	AI8	Lenosky, T. *et al.*, *Measurements of DMD-Challenged Fibers at 1310nm and 1Gb/s Data Rate*, IEEE 802.3ae - Equalization Ad Hoc Group, January 10, 2001, 21 pages.
JP	AJ8	Liu, M-K. and Modestou, P., "Multilevel Signaling and Pulse Shaping for Spectrum Efficiency in Subcarrier Multiplexing Transmission," *IEEE Journal of Lightwave Technology*, IEEE, Vol. 12, No. 7, pages 1239-1246.
JP	AK8	Olshansky, R. *et al.*, "Subcarrier Multiplexed Coherent Lightwave Systems for Video Distribution," *IEEE Journal on Selected Areas in Communications*, IEEE, Vol. 8, No. 7, September 1990, pages 1268-1275.
JP	AL8	Olshansky, R. *et al.*, "Subcarrier Multiplexed Lightwave Systems for Broadband Distribution," *IEEE Journal of Lightwave Technology*, IEEE, Vol. 7, No. 9, September 1989, pages 1329-1341.
JP	AM8	Otte, S. and Rosenkranz, W., "A Decision Feedback Equalizer for Dispersion Compensation in High Speed Optical Transmission Systems," *International Conference on Transparent Optical Networks*, IEEE, 1999, pages 19-22.
JP	AN8	Parhi, K. *et al.*, *Parallel Implementation of the DSP Functions of the PAM-5 10Gb/s Transceiver*, IEEE 802.3ae Task Force, March 2000, 12 pages.

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	AA9						
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	AF9						Yes No
	AG9						Yes No
	AH9						Yes No

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JP	AI9	Peral, E. et al., Measurements of time variation in DMD-challenged multimode fiber at 1310nm for 10GE equalizer applications, IEEE P802.3ae Equalization Ad Hoc, IEEE, March 2001, 19 pages.
JP	AJ9	Personick, S.D., "Baseband Linearity and Equalization in Fiber Optic Digital Communication Systems," Bell System Technical Journal, American Telephone and Telegraph Company, Vol. 52, No. 7, September 1973, pages 1175-1194.
JP	AK9	Personick, S.D., "Receiver Design for Digital Fiber Optic Communication Systems, I," Bell System Technical Journal, American Telephone and Telegraph Company, Vol. 52, No. 6, July-August 1973, pages 843-874.
JP	AL9	Personick, S.D., "Receiver Design for Digital Optic Systems," National Telecommunications Conference, IEEE, Atlanta, Georgia, November 26-28, 1973, Vol. 1, pages 8E-1 - 8E-4.
JP	AM9	Vorenkamp, P. et al., Analog Interface for 10-Gb/s Ethernet, IEEE 802.3ae Task Force, March 2000, 13 pages.
JP	AN9	Winters, J. and Gitlin, R., "Electrical Signal Processing Techniques in Long-Haul Fiber-Optic Systems," IEEE Transactions on Communications, IEEE, Vol. 38, No. 9, September 1990, pages 1439-1453.

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	AD10						
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	AF10						Yes No
	AG10						Yes No
	AH10						Yes No

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JP	AI10	Winters, J. et al., "Reducing the Effects of Transmission Impairments in Digital Fiber Optic Systems," *IEEE Communications Magazine*, IEEE, June 1993, pages 68-76.
JP	AJ10	*Progress Report on Equalization of Multimode Fibers*, IEEE 802.3ae Ad Hoc Group on Equalization, January 12, 2001, 16 pages.
JP	AK10	Alderrou, D. *et al.*, *XAUI/XGXS Proposal*, IEEE 802.3ae Task Force, May 23-25, 2000, 28 pages.
JP	AL10	Winters, J.H. and Gitlin, R., "Electrical Signal Processing Techniques in Long-Haul, Fiber-Optic Systems," *IEEE International Conference on Communications*, IEEE, Vol. 1, April 16-19, 1990, pages 0397-0403.
	AM10	
	AN10	

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